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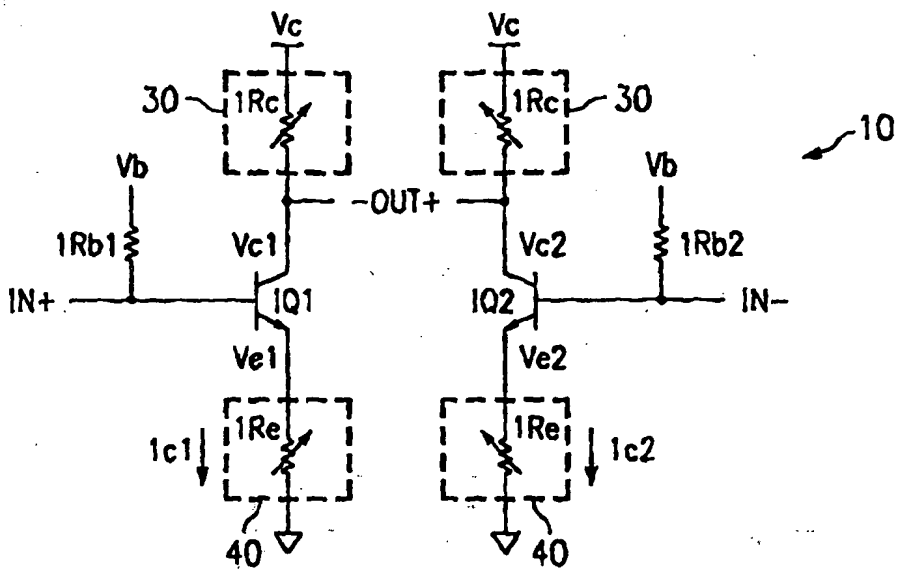
(54) Title: HIGHLY LINEAR VARIABLE-GAIN LOW NOISE AMPLIFIER

(57) Abstract

A highly linear variable-gain low noise amplifier is constructed using a transistor pair having variable gain control. The gain of the transistor pair is achieved by a segmented resistor having controllable PMOS (or NMOS) components. The circuit includes a variable voltage source and operates to handle wideband radio transmissions via broadcast or cable.



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HIGHLY LINEAR VARIABLE-GAIN LOW NOISE AMPLIFIER

TECHNICAL FIELD OF THE INVENTION

This invention relates to amplifier circuits and to amplifiers which are used in tuners and even more specifically to such amplifiers where variable-gain low noise amplification is required.

BACKGROUND OF THE INVENTION

U.S. Patent 5,737,035 dated April 7, 1998, shows a tuner circuit. The front end of such a tuner requires a broadband, highly linear Variable-gain Low Noise Amplifier (VLNA). The VLNA's input comes from either an antenna for wireless broadcasts or from a coaxial cable for cable transmission. The output of the VLNA supplies the input of the first up-converting mixer. The noise figure specification for the VLNA is highly critical, and has the highest impact on the overall noise figure of the system. Non-linearities of the amplifier also have a large effect on the proper operation of the tuner.

LNA's are typically used to meet cellular requirements, which are narrow-band. However, a television tuner must receive carriers from 50 MHZ to over 860MHz. A narrow bandwidth system also has less stringent linearity specifications because fewer intermodulation distortion products fall in-band. Finally, because the incoming signal power to a tuner can vary by many orders of magnitude, there is a need for an LNA whose gain is continuously-variable. The gain variability function adds noise, distortion, and complexity to the LNA.

Accordingly, there exists a need in the art for a low noise amplifier which can handle a wide frequency range as well as a wide amplification range.

A further need exists in the art for such a circuit which can be constructed on a single substrate and which will not be effected by, nor produce, noise injection.

SUMMARY OF THE INVENTION

These and other objects, features and technical advantages are achieved by a system and method which meets the noise, linearity, and gain ranges required in wide band tuners by using a segmented resistor and MOS structure in the signal path to vary the gain of a bipolar (or MOS) transistor amplifier. The system includes a method for both biasing the device and controlling the gain using a differential voltage input. Both PMOS, and NMOS transistors are used and operated in their triode mode to preserve linearity and low noise. The circuit operates for transmission signals received via air wave broadcast or via cable and can handle wide ranges of amplification requirements as well as intermodulation constraints.

It is a technical feature of my invention to provide a VLNA which utilizes a pseudo differential structure to reduce the effects of on-chip substrate injection and supply line fluctuations.

It is another technical feature of my invention to provide a circuit where the gain of the amplifier changes in a linear and predictable fashion with the controlling voltage input.

It is a further technical feature of my invention that such a circuit is constructed to produce a large gain range, having low noise, capable of operating across a wide band- width.

It is a further technical feature of my invention to provide such a circuit and method which is self biasing.

It is a further technical feature of my invention to provide such a circuit which will operate with circuits which require either a high constant output intercept or a high constant input intercept.

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily

utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 shows the overall bipolar transistor circuit of the amplifier;

FIGURE 2 is a graph showing the effects of varying the effective resistances of the circuit of FIGURE 1;

FIGURES 3 and 4 show the details of the segmented resistors of FIGURE 1; and

FIGURE 5 shows the details of the variable voltage source used with FIGURE 1.

FIGURE 6 shows a graph of control voltage versus differential control voltage input (gain control); and

FIGURE 7 shows the circuitry to accomplish the voltages shown in FIGURE 6.

DESCRIPTION OF THE INVENTION

The preferred embodiment of the invention employs a variation of a resistively-loaded NPN transconductance pair, 10, which includes transistors 1Q1 and 1Q2, as seen in Figure 1. As shown, both 1Re and 1Rc are continuously variable, to change the overall gain of the block. The voltage gain, A, is given by Equation 1, where "gm" refers to the transconductance of transistors 1Q1 and 1Q2.

$$A = \frac{1Rc}{1/gm + 1Re} \qquad \text{(Eq. 1)}$$

As can be seen, if the gm of the transistors is high enough, A is set by 1Rc/1Re. This allows the gain to be affected by varying either of these quantities, depending on specific desired qualities.

To reach maximum gain (Amax), resistor 1Rc is placed at its maximum value and resistor 1Re at its minimum. Gain reduction from Amax is accomplished by first increasing 1Re and then decreasing 1Rc. Varying these resistances produces other effects, as well.

For a given bias current through transistors 1Q1 and 1Q2, increasing 1Re decreases gain. Additionally, the Third-order Output Intercept Point (OIP3), which is a chief measure of linearity, remains relatively unaffected, while the Third-order Input Intercept Point (IIP3) increases. The noise figure of the device increases approximately one-half dB per dB of gain decrease.

Decreasing 1Rc decreases gain for a given bias current, and also reduces OIP3. However, IIP3 remains constant, while the noise figure increases a full dB per dB of gain decrease.

As can be seen in FIGURE 2, these behaviors cause distinctly different operating characteristics, depending on the gain selected. Region One behavior is exhibited while changing 1Re, while Region Two has 1Rc changing.

These two regions define two different applications for the tuner system as a whole. When the VLNA is supplied by a cable system, a multitude of carriers exist at its input, each with a similar limited power range. These multiple signals cause a large number of possible cross-modulated products, requiring very high output linearity, or OIP3, in the amplifier. Region One is defined such that it encompasses the range of power supplied from different cable systems.

When the VLNA is fed by an antenna, the amplifier must deal with far fewer carriers which are typically tightly regulated as to channel spacing and power, such that channel-to-channel interference is reduced thereby reducing the need for high linearity in the front end. A single channel, however, may contain much higher power than would be seen in a cable system thereby requiring a much lower level of gain. In this case the noise figure may be degraded by a larger amount, but a larger input linearity, or IIP3, must be maintained to avoid input compression. Region Two shows these characteristics.

The above observations about input and output intercept show general trends that will occur if the 1Rc and 1Re resistances are varied linearly, and if the resistors themselves remain non-distortive. The distortion due to the non-constant gm of the bipolar transistors will then dominate. However, anything with a transconductance that can be changed, i.e. 1Rc and 1Re, will be an active device, and have non-linearities of its own which must be controlled. While simple in concept, changing 1Rc and 1Re in an analog and predictable manner is quite difficult. As will be discussed in more detail hereinafter, the circuit uses a network of resistors and MOS devices to overcome this difficulty.

FIGURES 3 and 4 illustrate a preferred embodiment of resistors 1Rc and 1Re, respectively, which are variable, highly linear resistors. The nodes "Ve" and "Vc" correspond to the respective points in Figure 1. The control voltages Vp1, Vp2, Vp3, change the effective resistance of 1Rc by changing the gate voltages of PMOS devices 3Mp1, 3Mp2, 3Mp3, etc., and voltages Vn1, Vn2, Vn3, etc., likewise control 1Re (FIGURE 4). All subsequent discussion will describe 1Re, which uses NMOS transistors. The operation of 1Rc (Figure 3) may be understood by inverting the sense of the described control voltages Vp1, Vp2, Vp3, etc. (discussed with respect to FIGURES 6 and 7).

To set 1Re to its minimum resistance, all of the Vnx (when x can be any number 1, 2, 3, etc.) control lines are set to the highest available voltage. Due to bias conditions on Ve and the choice of values of Rnx, all of the MOS devices will be in a triode mode of operation. This gives a predictable drain-to-source resistance, inversely proportional to the gate voltage. Equation 2 provides a first order approximation of the equivalent resistance Rds provided by an NMOS, where Vth is the threshold voltage of the device, and C is a constant depending on process and transistor geometry.

$$Rds = \frac{1}{C * (Vnx - Vth)} \qquad \text{(Eq. 2)}$$

The resistance of 1Re is increased by changing the Vnx control lines in a successive manner. First, Vn1 is gradually reduced, then Vn2, then Vn3, etc., so as to reduce the voltage Vnx thereby increasing the effective resistance of the MOS device. But, the overall resistance is also affected by resistor Rnx, which has several effects. By limiting the contribution of total resistance of the MOS devices, it reduces the sensitivity of resistor 1Re to the control voltage, reduces the effect of the MOS's nonlinearity, and helps confine the transistors to the triode mode of operation.

FIGURE 6 shows the method of changing the Vnx control lines. 1Re's resistance is increased by changing the Vnx control lines in a successive manner. When reducing the amplifier's gain from its maximum point, first Vn1 is gradually reduced, then Vn2, then Vn3, etc., continually increasing 1Re's effective resistance. 1Rc's effective resistance is decreased after 1Re reaches its effective maximum by subsequently reducing the Vpx control lines. FIGURE 6 illustrates the response of the gain control circuitry to a differential control voltage.

FIGURE 7 shows a simplified diagram of the control circuitry for the voltages show in FIGURE 6. As shown, the control signal is applied to a fully differential amplifier 7Ad1 with gain Ks, which produces signal Vc. Amplifier 7Ad1 sets the sensitivity of the VLNA's gain to the applied differential control voltage Vcontrol. A larger Ks makes the VLNA's gain more sensitive with respect to Vcontrol.

Control voltage Vc is then distributed to separate amplifiers, 7An1 to 7Ap3, each controlling a Vnx or Vpx control line contained in the VLNA amplifier core. Each amplifier has an individual input offset voltage represented by a discrete voltage source at its input. The offset voltages are increased successively, starting with amplifier 7An1 and offset voltage Von1, and ending with amplifier 7Ap3 with offset Vop3. The gradually increasing offset voltages set the point where each control line will begin to change, or "breaks".

Also note that each amplifier has an individual gain Knx or Kpx , which sets the slope of the corresponding control line Vnx or Vpx during its transition. The amplifiers have a high output swing (from ground to Vcc) to correctly drive the MOS gates they control.

Returning now to FIGURE 1, the steady-state bias current 1c1 and 1c2 through transistors 1Q1 and 1Q2 is determined by the value of 1Re and the voltage applied at Vb. If Vb is set to a constant value, 1c1 will be reduced as 1Re is increased. This would further reduce the gain of the amplifier (gm would decrease) and reduce OIP3. To keep a constant OIP3, a constant bias current must be maintained. As a result, when changing 1Re, Vb must be changed appropriately.

FIGURE 5 shows the circuit which generates voltage Vb. Resistors 5Rb, 5Re and transistor 5Q1 are sized to match similar components in the circuit of FIGURE 1. Current 51c is the desired bias current. The actual current 1c1 and 1c2 may differ slightly due to matching of the devices. Buffer amplifier 501 drives Vb, with 5Vb as its input.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS

1. The method of adjusting the gain of a linear amplifier, wherein the amplifier includes at least a pair of transistors, said method comprising the steps of:

adjusting the AC current flow through the transistor pair in a controlled manner so as to maintain either the OIP3 or the IIP3 constant; and

adjusting the bias conditions (voltages and current) through the transistor pair consistent with the AC current change through the transistor pair.

2. The method of claim 1 wherein said first adjusting step includes the step of:

sequentially adding into the circuit path of said transistors an impedance value including one or more resistors, each said resistor having associated therewith a MOS device operable for changing the effective resistance of said associated resistor, wherein said sequentially adding step includes the step of varying the gate voltage of said MOS device to control the effective resistance of said device.

3. The method of claim 2 wherein said transistor pair are bipolar transistor pairs and wherein said circuit path includes both the emitter path and the collector path and wherein said sequentially adding step includes the step of:

selecting into which path said impedance is to be changed.

4. The method of claim 2 wherein said transistor pair are MOS transistors and wherein said circuit path includes both the source path and the drain path and wherein said sequentially adding step includes the step of:

selecting into which path said impedance is to be changed.

5. A linear variable gain amplifier for use in a RF tuner, said amplifier comprising:

a pair of transistors; and

means for adjusting the current flow through the transistor circuit path so as to vary the gain of said amplifier, while maintaining either the OIP3 or the IIP3 of said amplifier at a constant level.

6. The amplifier of claim 5 wherein said adjusting means includes:

means for sequentially adding into said circuit path of said transistors an impedance value including one or more resistors, each said resistor having associated therewith a MOS device operable for changing the effective resistance of said associated resistor.

7. The amplifier of claim 6 wherein said sequentially adding means includes:

means for varying the gate voltage of said MOS device to control the effective resistance of said device.

8. The amplifier of claim 7 wherein said transistor pair is a bipolar transistor pair and wherein said circuit path includes both the emitter path and the collector path and wherein said sequentially adding step includes:

means for selecting into which path said impedance is to be added.

9. The amplifier of claim 7 wherein said transistor pair is a MOS transistor and wherein said circuit path includes both the source path and the drain path and wherein said sequentially adding step includes:

means for selecting into which path said impedance is to be added.

10. The amplifier of claim 5 wherein said amplifier is capable of handling a wide range of input frequencies.

11. The amplifier of claim 10 wherein said wide range is 50-860 MHZ.

12. An amplifier capable of operating in either a first region where high output linearity is required or in a second region where a high input linearity is required, said amplifier comprising:

a transconductance stage;

a first controllable impedance selectively variable within a range to operate said amplifier in said first region;

a second controllable impedance selectively variable within a range to operate said amplifier in said second region; and

a plurality of transistors for controlling the effective values of said first and second impedances.

13. The amplifier in claim 12 wherein said plurality of transistors are MOS devices.

14. The amplifier in claim 13 wherein said transconductance stage is a pair of transistors.

15. The amplifier in claim 14 wherein said first and second impedances are pairs of impedances respectively connected to said transistor pairs.

16. The amplifier in claim 14 wherein said transistor pair is a bipolar transistor pair and wherein said first impedance is connected in the emitter circuits of said transistor pair.

17. The amplifier in claim 16 wherein said second impedance is connected in the collector circuits of said transistor pair.

18. The amplifier in claim 14 wherein said transistor pair is a MOS transistor pair and wherein said first impedance is connected in the source path of said MOS transistor pair.

19. The amplifier in claim 18 wherein said second impedance is connected in the drain path of said MOS transistor pair.

20. The amplifier in claim 13 further including circuits for varying the gate voltage of said MOS devices to control the effective impedance of said controllable impedance.

21. The amplifier in claim 12 wherein said impedance is resistive.

22. The amplifier in claim 14 further including circuitry to bias said amplifier.

23. The amplifier in claim 12 wherein said first region is capable of amplifying signals received over a cable and wherein said second region is capable of amplifying signals received from a broadcast reception antenna.

24. The method of amplifying signals received either from cable channels or from antenna channels, said cable channels requiring high output linearity and said antenna channels requiring high input linearity; said method including the steps of:

passing said signals through a gain stage of an amplifier; and

selectively varying the impedance in the gain circuit path in a highly controlled fashion so as to achieve the desired result.

25. The method of amplifying in claim 24 wherein said gain stage includes a pair of bipolar transistors and achieve said selectively varying step includes:

separately changing resistance to the emitter circuit for cable signals; and

separately changing resistance to the collector circuit to antenna signals.

26. The method of amplifying in claim 24 wherein said gain stage includes a pair of MOS transistors and wherein said selectively varying step includes:

separately changing resistance to the source path for cable signals; and

separately changing resistance to the drain path for antenna signals.

27. A variable gain amplifier, said amplifier comprising:

means for decreasing said gain of said amplifier from a high value said means operable for holding the OIP3 of said amplifier constant while the IIP3 of said amplifier increases; and

means below a transition point for continuing to decrease said gain while maintaining a constant IIP3 and while decreasing said OIP3.

28. The amplifier of claim 27 further comprising:

means for gradually degrading the noise figure of said amplifier as said gain is decreased.

29. The amplifier of claim 28 wherein said noise figure degradation is less per unit of gain decrease above a transition point than it is below said last-mentioned transition point.

30. The amplifier of claim 28 wherein the slope of said degradation above said transition point is less than 1 dB of noise figure for each db of gain decrease.

31. The amplifier of claim 27 wherein said transition point is at 0 dB of gain.

32. The amplifier of claim 27 wherein said high value is greater than 15 dB.

33. The amplifier of claim 27 wherein said gain is decreased to less than -20 dB.

34. The amplifier of claim 27 wherein said constant OIP3 is greater than 70 dBmV

35. The amplifier of claim 27 wherein said constant IIP3 is greater than 55 dBmV.

36. The method of operating an amplifier, said method including the steps of:

decreasing the gain of said amplifier from a high value while holding the OIP3 of said amplifier constant while the IIP3 of said amplifier increases; and

below a transition point continuing to decrease said gain while maintaining a constant IIP3 and while decreasing said OIP3.

37. The method of claim 36 further comprising the step of:

gradually degrading the noise figure of said amplifier as said gain is decreased.

38. The method of claim 37 wherein said noise figure degrading is less per unit of gain decrease above a transition point than it is below said last-mentioned transition point.

39. The method of claim 37 wherein the slope of said degradation above said transition point is less than 1 dB of noise figure for each dB of gain decrease.

40. The method of claim 36 wherein said transition point is at 0 dB of gain.

41. The method of claim 36 wherein said high value is greater than 15 dB.

42. The method of claim 36 wherein said gain is decreased to less than -20 dB.

43. The method of claim 36 wherein said constant OIP3 is greater than 70 dBmV.

44. The method of claim 36 wherein said constant IIP3 is greater than 55 dBmV.

FIG. 1

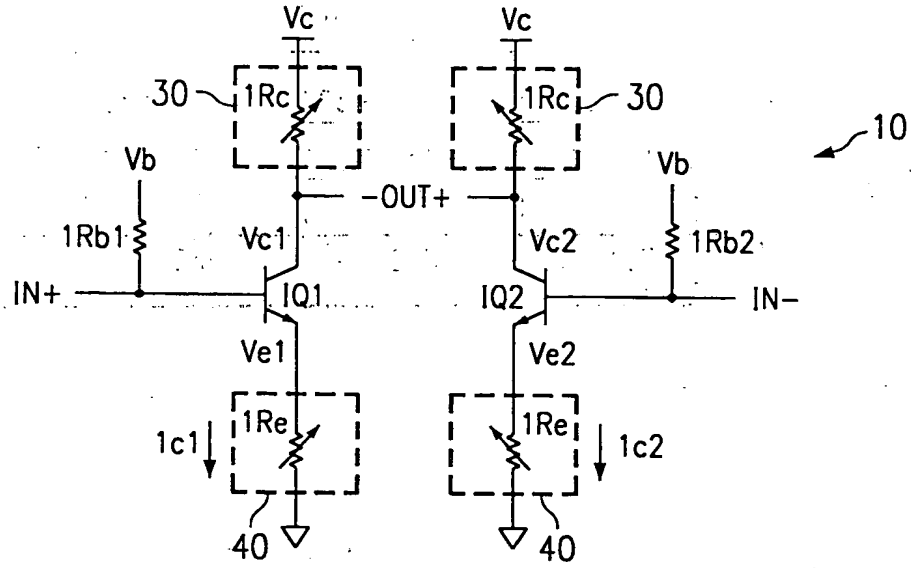


FIG. 2

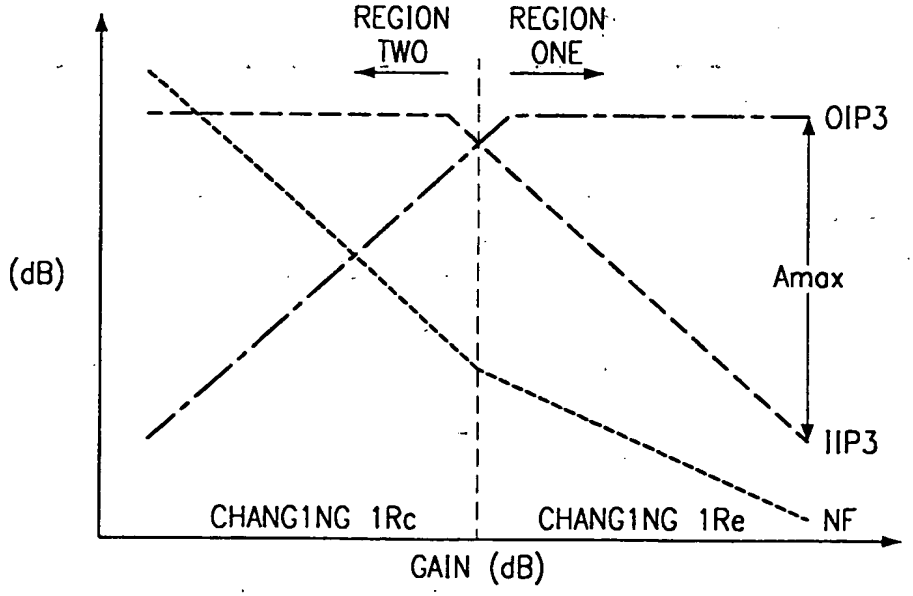


FIG. 3

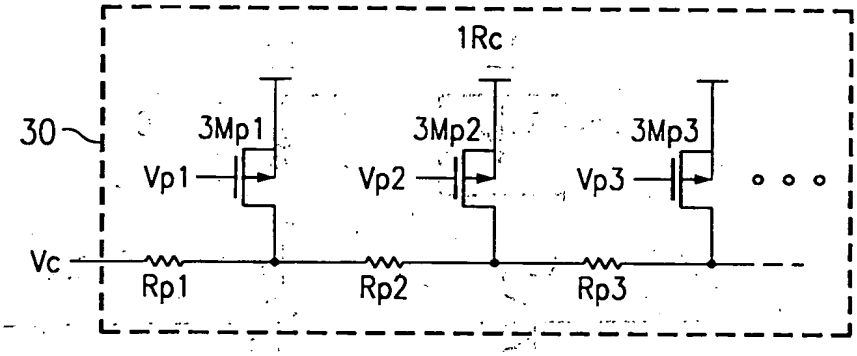


FIG. 4

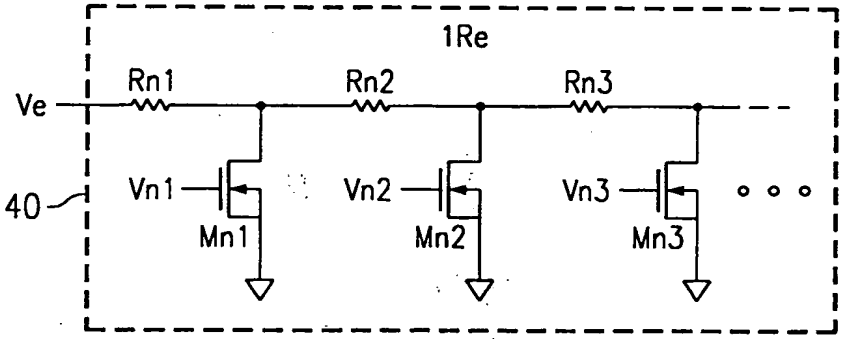
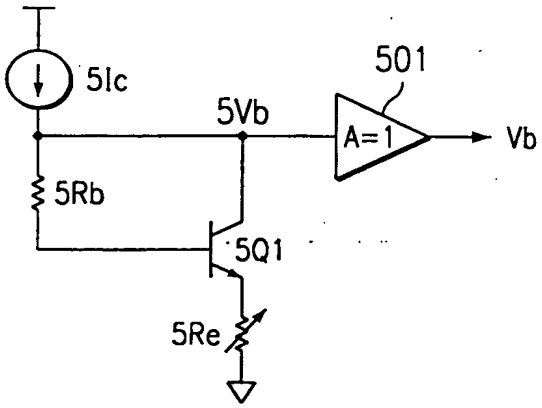


FIG. 5



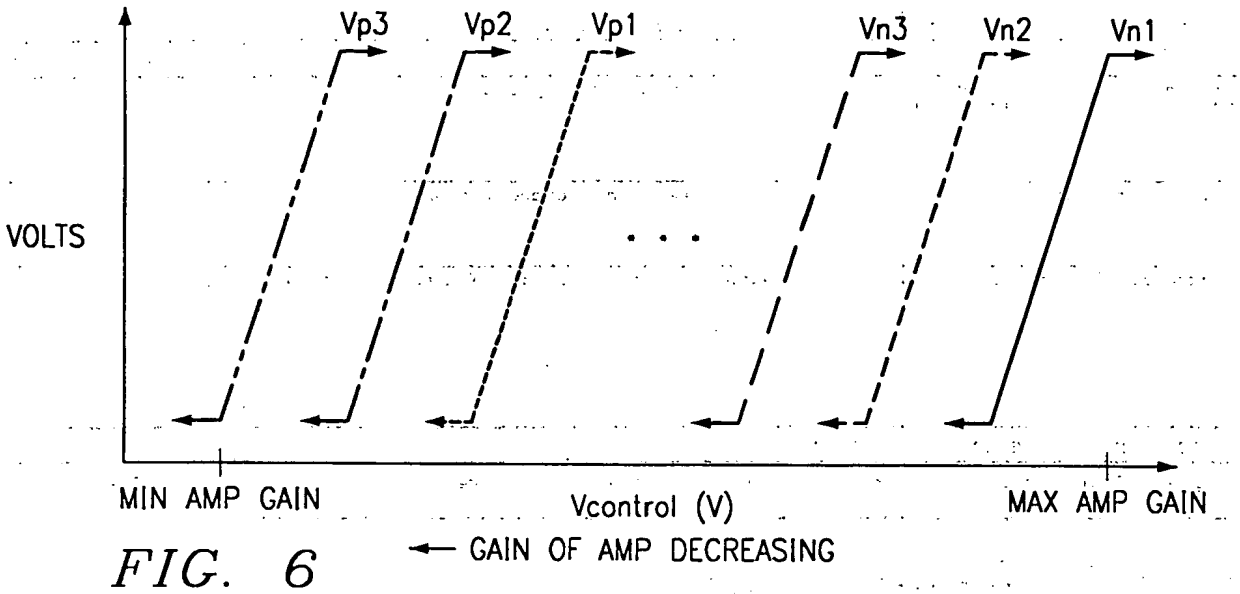


FIG. 6

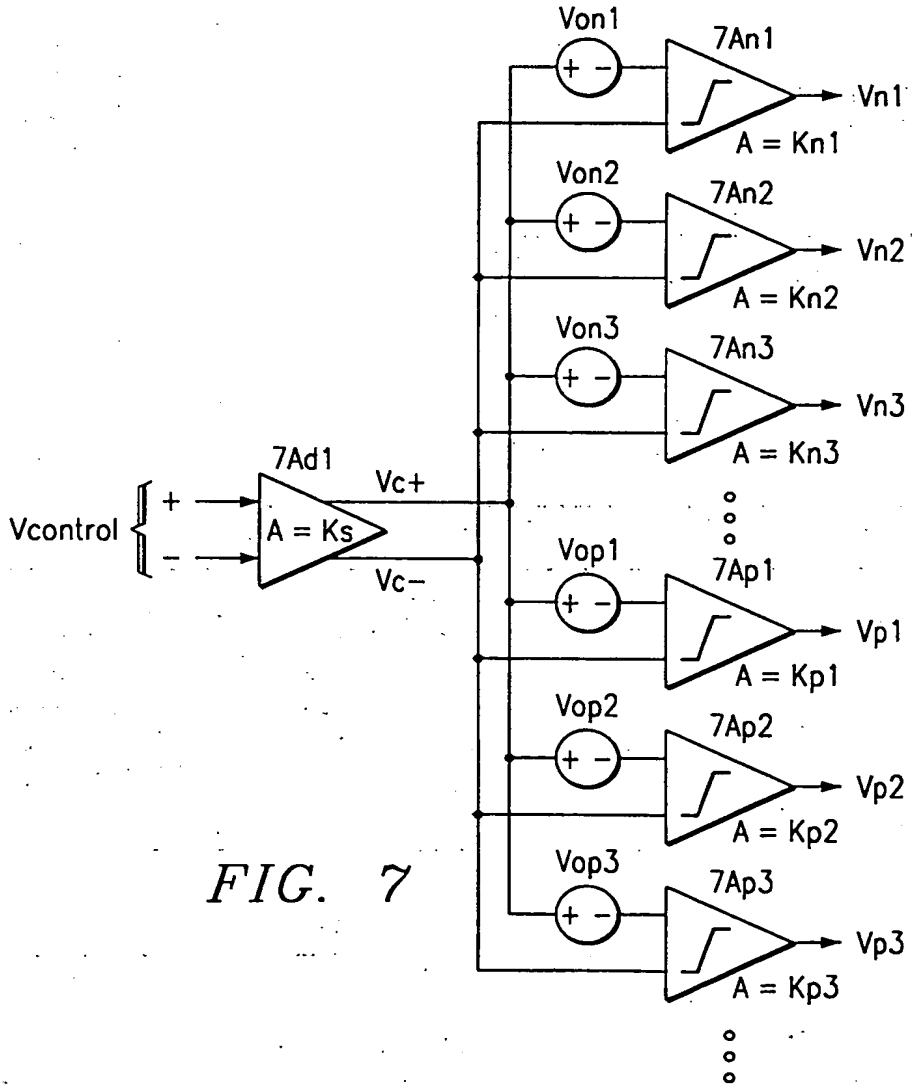


FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/23053

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/18 H03G1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 344 044 A (HARFORD JACK R) 10 August 1982 (1982-08-10)	1,5, 10-12, 23-25, 27,28, 30-37, 39-44
A	the whole document	2,3,6,8, 13-17, 21,22, 26,29,38
A	JP 60 096012 A (MATSUSHITA DENKI SANGYO KK) 29 May 1985 (1985-05-29) abstract	1-3,5-8, 10-16, 18,20, 21,24, 25,27,36

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 415 864 A (BOEKE WOUTER M) 15 November 1983 (1983-11-15) the whole document	1,2,4-7, 9-15,17, 19-22, 24,26, 27,36
A	EP 0 514 655 A (MATSUSHITA ELECTRIC IND CO LTD) 25 November 1992 (1992-11-25) abstract figure 4 column 15, line 22 -column 16, line 10 column 1, line 1 -column 11, line 31 figure 1	1,2,4-7, 9-15,18, 20-24, 26-44

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 99/23053

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4344044 A	10-08-1982	NONE	
JP 60096012 A	29-05-1985	NONE	
US 4415864 A	15-11-1983	NL 8001117 A	16-09-1981
		CA 1157921 A	29-11-1983
		DE 3106575 A	04-02-1982
		FR 2476938 A	28-08-1981
		GB 2070359 A,B	03-09-1981
		HK 75484 A	12-10-1984
		JP 1033047 B	11-07-1989
		JP 1550051 C	09-03-1990
		JP 56132008 A	16-10-1981
EP 0514655 A	25-11-1992	JP 2938999 B	25-08-1999
		JP 4345305 A	01-12-1992
		DE 69224676 D	16-04-1998
		DE 69224676 T	17-09-1998
		KR 9606537 B	17-05-1996
		US 5210504 A	11-05-1993